INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 00/02145

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G02B6/132

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G02B H01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 855 255 A (GOODHUE WILLIAM D) 8 August 1989 (1989-08-08) abstract; figure 9 column 2, line 21 - line 33 column 10, line 50 - line 53	1,5,6
Y	---	2-4
Y	MOERMAN I ET AL: "A review on fabrication technologies for the monolithic integration of tapers with III-V semiconductor devices" IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, DEC. 1997, IEEE, USA, vol. 3, no. 6, pages 1308-1320, XP002146284 ISSN: 1077-260X page 1314, column 2, line 12 - line 18	2-4

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 August 2000	13/09/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Jakober, F

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	COLAS E ET AL: "IN SITU DEFINITION OF SEMICONDUCTOR STRUCTURES BY SELECTIVE AREA GROWTH AND ETCHING" APPLIED PHYSICS LETTERS,US,AMERICAN INSTITUTE OF PHYSICS. NEW YORK, vol. 59, no. 16, 14 October 1991 (1991-10-14), pages 2019-2021, XP000257432 ISSN: 0003-6951 the whole document	4
A	VEUHOFF E: "Potential of MOMBE/CBE for the production of photonic devices in comparison with MOVPE - Appl. Phys" JOURNAL OF CRYSTAL GROWTH,NL,NORTH-HOLLAND PUBLISHING, AMSTERDAM, vol. 188, no. 1-4, 1 June 1998 (1998-06-01), pages 231-246, XP004148350 ISSN: 0022-0248 the whole document	1-6
A	LORKE A ET AL: "TAPERED GaAs QUANTUM WELLS AND SELECTIVELY CONTACTABLE TWO-DIMENSIONAL ELECTRON GASES GROWN BY SHADDOW MASKED MOLECULAR-BEAM EPITAXY" JOURNAL OF APPLIED PHYSICS,US,AMERICAN INSTITUTE OF PHYSICS. NEW YORK, vol. 77, no. 7, 1 April 1995 (1995-04-01), pages 3578-3580, XP000501596 ISSN: 0021-8979 the whole document	1-6

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 00/02145

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4855255 A	08-08-1989	WO 8909490 A	05-10-1989
		US 4999316 A	12-03-1991

METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

The invention relates to a method of fabricating a semiconductor devicewith a tapered pitaxial layer.

Opto-electronic systems contain optical fibres and opto-electronic semiconductor devices such as lasers, amplifiers, modulators, detectors and switches. The size and shape of the optical modes supported by optical fibres are significantly different to those within opto-electronic semiconductor devices, and this results in modal mismatch and high optical losses when optical radiation is coupled between such devices and fibres.

One technology which reduces such optical losses involves the use of a microlens placed between the opto-electronic semiconductor device and the optical fibre. The microlens changes the size of the optical mode output by the opto-electronic semiconductor device or optical fibre, but not the shape of the mode. Another technology involves the use of an optical mode-converting waveguide placed between the opto-electronic semiconductor device and the optical fibre. Both of these technologies demand very high alignment tolerances with the result that the alignment of the components can represent the most significant part of the total cost of an opto-electronic system.

A third technology which reduces coupling losses involves the use of opto-electronic semiconductor devices having output waveguides with a two-dimensional tapered thickness profile between the active part of the device and the output facet. This tapering of the output waveguide allows the relatively small (0.5 to 2.0 μm) and sometimes highly asymmetric optical mode from the active part of an opto-electronic semiconductor device to be closely matched to the larger (6 to 10 μm), circularly symmetric optical mode supported by an optical fibre.

Lateral tapering of the output waveguide of an opto-electronic semiconductor device, i.e. tapering in a plane parallel to a substrate surface, may be achieved using known s miconductor processing techniques such as ph tolithography and chemical tching. This is carried out after epitaxial growth of the wafer from which the device is made. Tap ring the core layer of a waveguide in a plane perpendicular to the plane of

epitaxial layer on which it is grown is more difficult and involves controlling the thickness of the core layer during wafer growth.

Methods currently used for producing vertically tapered and flared semiconductor optical waveguides are described by Moerman in IEEE Journal of Selected Topics in Quantum Electronics, Volume 3 , Number 6, pp 1308 - 1320 and may be classified under three main headings, as follows:

Etching and re-growth techniques:

In these techniques, epitaxial growth of the wafer is stopped after deposition of the core layer of the waveguide. The wafer is then removed from the wafer growth apparatus and the core layer is etched to produce the required taper profile. The wafer is then replaced in the growth apparatus and the upper guiding layer is grown over the etched core layer. These techniques have the following disadvantages. First, the overall processing is complex and time-consuming. Second, removal of the partially-grown wafer from the growth apparatus and etching the waveguide core layer introduces contamination into the waveguide, increasing optical losses and reducing yield. Third, these methods have very low reproducibility. In one such method, known as dip-etching, it not possible to process the whole surface of a wafer.

Impurity-induced disordering:

This is a technique for producing vertically tapered waveguides starting with a waveguide in which the core layer has a uniform thickness. This technique is limited in that the initial uniform waveguide must have a core layer consisting of a multiple quantum-well region. Zinc is diffused into the waveguide through the upper guiding layer and penetrates the core layer to depth which varies with lateral position, i.e. position in the plane of the epitaxial layers. Where zinc has diffused, the refractive index of the core layer is reduced to that of the guiding layers, producing vertical tapering of the waveguide. This technique has low reproducibility, and the resulting waveguides have significant optical loss in the regions where zinc diffusion occurs. It is also limited in respect of the material systems that may be used.

Epitaxial techniques:

Several techniques exist in which the tapered core layer and upper guiding layer of a waveguide may be grown in a single step. For example , a temperature gradient

introduced in the plane of a wafer consisting of a substrate and a lower guiding layer during the growth of the core layer by molecular beam epitaxy (MBE) may be used to control the thickness of that layer. In this technique it is very difficult to control the compositional uniformity of ternary and quaternary compounds across the temperature gradient and materials having a low melting point or requiring a high growth temperature may have a narrow range of suitable growth temperatures. This places limits on the temperature gradients that may be employed.

Another epitaxial technique is known as "growth-on-a-ridge". By standard etching methods a ridge of varying width may be produced on a wafer comprising a substrate and a lower guiding layer. Due to surface diffusion properties of metal-organic vapour-phase epitaxy (MOVPE), the growth rate of the remaining waveguide layers increases as the width of the ridge decreases, producing a tapered waveguide. This technique involves complicated and time-consuming wafer processing before epitaxial growth of the core and upper guiding layers can take place.

Yet another epitaxial technique is shadow-mask MOVPE growth using a dielectric mask. In this technique, a patterned dielectric mask is deposited onto a wafer. During MOVPE epitaxial growth, deposition takes place through a window in the shadow mask. The lateral thickness of the layer deposited underneath the shadow mask may be controlled by varying the lateral dimensions of the window, the distance between the mask and the substrate, and the reactor pressure. This technique involves an additional growth step of growing the dielectric mask and an additional processing step to remove it. It also involves processing steps to pattern the mask which involve considerable delay and may leave the surface contaminated. Although a mechanical shadow mask may be used instead of a dielectric mask, MOVPE growth inevitably results in compositional non-uniformity within the tapered layer due to the unequal diffusion lengths of the reaction gases in MOVPE growth. This results in refractive index non-uniformity within the tapered layer which adversely affects the guiding of light within that layer. Also, exposure of the wafer to the atmosphere during mask insertion and removal may result in contamination of the wafer. A further disadvantag is that deposition of material on the mask its lf necessitates mask cleaning or replacement.

It is an object of the invention to provide an alternative process for fabricating a semiconductor optical slab-waveguide.

The invention provides a method of fabricating a semiconductor device including a step of growing at least one tapered epitaxial layer upon a supporting surface, characterised in that the at least one tapered epitaxial layer is grown by chemical beam epitaxy (CBE) with a taper in a plane inclined to the supporting surface.

The invention makes it possible to fabricate a waveguide incorporating a core layer which tapers continuously in a plane perpendicular to the plane of a substrate on which the waveguide is fabricated. In tapered waveguides grown by MOVPE, the core layer thickness first increases before tapering to the thin part of the core. This adversely affects the guiding properties and optical loss of the waveguide and is avoided in the present process. Furthermore, compositional inhomogeneities present in tapered regions of waveguides produced by MOVPE growth are avoided due to the absence of gas phase reactions in CBE growth. The present method makes it possible to avoid uncontrolled changes in thickness and refractive index during epitaxial growth that may affect the guiding properties of a waveguide or increase its optical loss.

The invention also provides a method of fabricating a semiconductor device characterised in that the at least one tapered epitaxial layer is grown with the taper in a plane perpendicular to the supporting surface using a mechanical shadow mask and a single epitaxial growth step.

As the tapered layer is produced entirely by epitaxial growth, the process is relatively simple and rapid, allowing relatively inexpensive production on an industrial scale. The method avoids contamination associated with processing a layer to obtain a layer tapered in a plane perpendicular to a surface supporting it. As there is no polycrystalline growth on the shadow mask during epitaxial growth, a shadow mask used in the process maintains its definition during the process and may be re-used without cleaning in further growth runs. This is in contrast to growth by MBE where significant polycrystalline growth occurs on the shadow mask causing unwanted shadowing effects.

The invention further provides a method of fabricating a semiconductor device characterised in that the at least one tapered epitaxial layer is grown in the same growth step as at least one untapered epitaxial layer.

The method provides improvements in the rate at which such devices may be produced and in the yield and quality of such devices.

When the process is employed to fabricate waveguides of aluminium gallium arsenide (AlGaAs) and gallium arsenide (GaAs) it preferably uses triethyl gallium (TEGa) or tri-isopropyl gallium (TIPGa) as the gallium source, the ethyl dimethylamine adduct of alane (EDMAAl) as the aluminium source and thermally-cracked arsine as the arsenic source. In order to reduce impurities in the growth crystal and so improve optical characteristics of the resulting device, the growth is preferably conducted at a temperature in the range 500 to 600 °C.

In the case of waveguides based on indium phosphide (InP) and indium gallium arsenide phosphide (InGaAsP) the process preferably uses trimethyl indium (TMIn), trimethyl gallium (TMGa), arsine and phosphine as the sources of indium, gallium, arsenic and phosphorus respectively.

In order that the invention may be more fully understood, embodiments thereof will now be described, by way of example only, with reference to the accompanying drawings in which:

Figures 1 to 4 show the principal stages in a process according to the invention for producing a semiconductor optical waveguide with a core layer which is tapered in two dimensions,

Figure 5 shows a vertical section of a mechanical apparatus used during production of the waveguide,

Figure 6 shows a vertical s ction of a shadow mask used in the process,

Figure 7 shows a plan view of the shadow mask, and

CLAIMS

1. A method of fabricating a semiconductor device including a step ofgrowing at least one tapered epitaxial layer upon a supporting surface, characterised in that the at least one tapered epitaxial layer is grown by chemical beam epitaxy with a taper in a plane inclined to the supporting surface.

2. A method according to Claim 1 characterised in that the at least one tapered pitaxial layer is grown with the taper in a plane perpendicular to the supporting surface using a mechanical shadow mask and a single epitaxial growth step.

3. A method according to Claim 2 characterised in that the at least one tapered epitaxial layer is grown in the same growth step as at least one untapered epitaxial layer.

4. A method according to Claim 2 or 3 characterised in that the mechanical shadow mask comprises a silicon wafer having etched apertures and an oxide film coating upon which deposition does not occur at temperatures used for growth by chemical beam epitaxy.

5. A method according to any preceding claim characterised in that the semiconductor device is a device in which radiation is guided.

6. A method according to Claim 5 characterised in that the semiconductor device is an optical waveguide.

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Commissioner
US Department of Commerce
United States Patent and Trademark
Office, PCT
2011 South Clark Place Room
CP2/5C24
Arlington, VA 22202
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 31 January 2001 (31.01.01)	
International application No. PCT/GB00/02145	**Applicant's or agent's file reference** IPD/P2844/1/WOD
International filing date (day/month/year) 02 June 2000 (02.06.00)	**Priority date** (day/month/year) 14 June 1999 (14.06.99)
Applicant MARTIN, Trevor et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

07 December 2000 (07.12.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer S. Mafla
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

ATENT COOPERATION TRE. Y

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92bis.1 and Administrative Instructions, Section 422)

To:

BOWDERY A.O.
Qinetiq Limited
IP Formalities
A4 Bldg., Cody Technology Park
Ively Road, Farnborough
Hampshire GU14 0LX
ROYAUME-UNI

Date of mailing (day/month/year)
02 November 2001 (02.11.01)

Applicant's or agent's file reference
IPD/P2844/1/WOD

IMPORTANT NOTIFICATION

International application No.
PCT/GB00/02145

International filing date (day/month/year)
02 June 2000 (02.06.00)

1. The following indications appeared on record concerning:

☐ the applicant ☐ the inventor ☐ the agent ☐ the common representative

Name and Address
THE SECRETARY OF STATE FOR DEFENCE
Defence Evaluation and Research Agency
A4 Building
Ively Road
Farnborough
Hampshire GU14 0LX
United Kingdom

State of Nationality: GB
State of Residence: GB
Telephone No.:
Facsimile No.:
Teleprinter No.:

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

☒ the person ☐ the name ☐ the address ☐ the nationality ☐ the residence

Name and Address
QINETIQ LIMITED
85 Buckingham Gate
London SW1 6TD
United Kingdom

State of Nationality: GB
State of Residence: GB
Telephone No.:
Facsimile No.:
Teleprinter No.:

3. Further observations, if necessary:
The agent's address has been changed accordingly.

4. A copy of this notification has been sent to:

☒ the receiving Office
☐ the International Searching Authority
☒ the International Preliminary Examining Authority
☐ the designated Offices concerned
☒ the elected Offices concerned
☐ other:

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland
Facsimile No.: (41-22) 740.14.35

Authorized officer
Maria Victoria CORTIELLO
Telephone No.: (41-22) 338.83.38

PATENT COOPERATION TREATY

RECD 12 SEP 2001

WIPO PCT

14

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
IPD/P2844/1/WOD		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB00/02145	02/06/2000	14/06/1999
International Patent Classification (IPC) or national classification and IPC G02B6/132		
Applicant THE SECRETARY OF STATE FOR DEFENCE		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 6 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
07/12/2000	12.09.2001
Name and mailing address of the international preliminary examining authority: European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016	Authorized officer Jakober, F Telephone No. +31 70 340 3652

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB00/02145

I. Basis f th r p rt

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:
Description, pages:

6-10	as originally filed	
1-5	with telefax of	11/04/2001

Claims, No.:

1-5	with telefax of	11/04/2001

Drawings, sheets:

1/5-5/5	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-5
	No:	Claims	
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-5
Industrial applicability (IA)	Yes:	Claims	1-5
	No:	Claims	

2. Citations and explanations
   see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

R Item V

Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

D1: US-A-4855255

D2: IEE Journal Of Selected Topics In Quantum Electronics, Dec. 1997, IEEE, Usa, 3(6), 1308-1320

D3: Applied Physics Letters,us,american Institute Of Physics. New York (14-10-1991), 59(16), 2019-2021

1. The application does not fulfill the requirements of Article 33(3) PCT because the subject-matter of independent claim 1 does not involve an inventive step. Document D1 discloses a method of fabricating a semiconductor taper waveguide on a substrate. Different method of deposition can be used. An example is given with molecular beam epitaxy (see figure 9a-9c and corresponding passages in the description). However, column 10, line 50 to 53 of the description specifies that the fabrication of the taper can also be caried out by chemical beam epitaxy. The taper is obtained by establishing a temperature gradient on the surface. This process can be relatively complex specialy when different designs have to be formed. But it is well-known to the skilled person to use masking technics, in particular mechanical masks, the later having the advantage to be easily placed on top of the substrate and easily removed, as explained in document D2 (page 1314, second column, lines 12-18 and figure 7(f)). The skilled person would therefore use mechanical masks to simplify the process of document D1.

2. Dependent claims 2-5 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of inventive step, the reasons being as follows:
- the use of a mechanical mask for the epitaxial growth in a single step of taper layers is a well known technique in the art (see for example document D2 page 1314, second column, lines 12 to 18).
- mechanical masks with an oxide coating to avoid epitaxial deposition on the

mask are also known in the art (see document D3).
- document D1 discloses a semiconductor taper optical waveguide.

Therefore, the application does not fulfill the requirements of article 33.3 PCT.

Re Item VII

Certain defects in the international application

1. Claim 2 should be dependent on claim 1.